


## Article

# A Single Transformer for Active Cell Equalization Method of Lithium-Ion Batteries with Two Times Fewer Secondaries than Cells

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**Abstract:** In this paper, the concept of active cell-balancing technique, by using a multiple-outputs double-forward converter for lithium-ion (Li-ion) batteries, is investigated. It controls two times more cells than secondaries, and it equalizes eight cells in a series. In this method, four secondaries can reasonably be wound with the same back electromotive force (EMF). This means a low pin count on the transformer and a low bill of materials (BOM). The bridge uses four N-channel MOSFETs as switches, which means two times fewer transistors than cells, resulting in fewer switching losses. This scheme is applied for controlling the minimum voltage among the cells of the lithium-ion battery. It uses a multi-winding transformer based on a forward double converter structure. Conventional schemes using a multi-winding transformer for electric vehicles (EVs) require an equal number of secondaries per cell. This scheme requires one secondary for two adjacent cells, thus the number of secondaries is reduced by a factor of two. Also, the redistribution of charge from a high cell to a low cell does not require many switching components and little intelligence to determine low cell voltage detection. The basic principle of this method is to use the overall battery pack voltage as a reference to supply individual cells, using a forward converter containing a transformer with a well-chosen winding ratio. The experimental and simulation results are performed to verify the feasibility of the proposed system.

**Keywords:** cell-balancing; double-forward converter; Li-ion; EMF; BOM; EV

## 1. Introduction

Lithium-ion batteries are widely used due to their low self-discharging rate, a high number of cycles, lower weight, no memory effects, and high energy density [1–5]. Therefore, they have many advantages and they are applied in many applications, such as electric vehicles (EVs), hybrid electric vehicles (HEVs), electric scooters (ESs), electric bikes, and uninterruptible power supplies (UPS) [6–8]. The applications may employ hundreds of Li-ion cells for modules, connecting them in series or in parallel to apply to high voltage and high capacity systems, such as electric vehicles and energy storage devices [9]. They cannot have equal characteristics as they use chemical energy [10,11]. However, manufacturing tolerances result in variations of the battery capacitance and internal resistance from cell to cell [12]. The problems of the capacity and resistance variation are increased by a different cell aging. This imbalance results in a reduction in the charge storage potential and the lifetime of the battery pack. With repeated charging and discharging cycles, each battery cell shows the voltage imbalance. Voltage imbalance is a major factor to deteriorate the performance and reliability of the battery pack, because of the decrease in the usable capacity due to low voltage battery cell and the explosion risk due to overcharging. Thus, battery equalizers are needed to ensure that all cells in a series-connected

battery string are fully charged or discharged. Many battery equalizers have been proposed in the last few years [13–22]. These applications are divided into a passive balancing technique and an active balancing technique.

The passive balancing technique connects resistors and switches to each battery cell and dissipates energy using resistors. They work based on removing the excess energy from the higher cells, by bypassing the current of the higher cells, until all the cells are at the same voltage level. On the other hand, the active balancing technique is used to overcome the problem of energy losses. It equalizes battery cells by transferring charge from higher cells to lower cells. The active balancing is divided into two categories such as charging pass type and multi-winding transformer type.

In the first type, energy is stored in a capacitor or an inductor through a switch to transfer charges to another cell [15,23]. The advantage of the capacitor type is that the circuit configuration is simple, but on the other hand, the disadvantage of this method is a long equalization time. The inductor balancing method has an advantage of fast equalization time [13,20], but the energy transfer is possible only between neighboring cells. Therefore, the balancing speed is slower as compared to the transformer balancing method. In the second type, the multi-winding transformer has an advantage that direct energy transfer is possible between non-adjacent battery cells [8,9,17,21,24–36]. The multi-winding transformer topology has a magnetic core with primary and multi-secondary windings for each cell. The advantage of this method can be expressed as very simple, easy to control, and low cost. In Figure 1 the circuit of the conventional multi-winding transformer balancing method is presented. This technique requires one secondary and one switch per cell, so the number of secondaries and switches are two times more compared to the proposed circuit shown. This means, more costs, more complicated circuits, and less efficient.

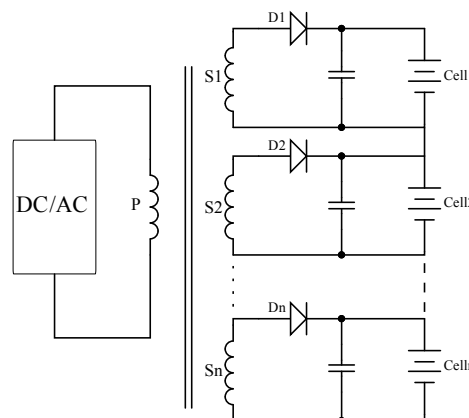


Figure 1. Conventional multi-winding balancing circuit method.

This paper proposes a direct balance circuit using a multi-winding transformer. Energy transfers from the total package to the low voltage cells. The main suitability of this paper is that the number of secondary windings is reduced by the factor of two by using a double-forward converter. It results in a cost-effective, more efficient, and less complicated circuit. Also, the number of switches is reduced, resulting in a simpler control and fewer losses.

## 2. The Proposed Multi-Winding Balancing Circuit

In this section, the concept of a multi-winding transformer with four secondaries for a battery with 8 cells by a double-forward converter will be explained and a proof of concept will be given through practical test results. The basic principle of this circuit is to use the overall battery pack voltage as a reference to supply individual cells, using a forward converter containing a transformer with a well-chosen winding ratio. When a cell drops below the voltage level of accompanying pack cells, an extra charge will be supplied to this cell from the entire battery pack. The transformer has a single primary winding and 4 secondary windings. In each of secondary winding, an equal induced voltage

is assumed. When an imbalance occurs, a current will flow proportional to the extent of the imbalance. On the primary side, this current will allow the detection of imbalance and a battery pack by-pass when the imbalance is critical. It has the advantage that each cell has not to be compared with a reference voltage, but that the principle relies on a transformer ratio.

The operational principle of this circuit is based on a double-forward converter. The double-forward aspect indicates the usage of both up and downsides of a primary signal for balancing. This means, a positive half-cycle is used to balance one half of the cells, while the negative half-cycle is used to balance the other half, as displayed in Figure 2. Assume that cell number 1 is at a lower voltage, while other cells are at a nominal voltage. Since all the cells surrounding cell number 1 are at a higher voltage, the transformed reference voltage will also be higher, allowing the balancing of cell number 1. By doing this, the number of secondary windings can be limited to 4. This means that they can be easily wound in a “wound one hand” secondary, where the symmetry allows an equal EMF in the windings. The forward transformer needs no air gap, so the EMF is quite equal among the windings. The positive-negative can be adjusted by the duty ratio if required. The transformer can be loaded with an asymmetric DC if sufficient dead time is given between each half period.

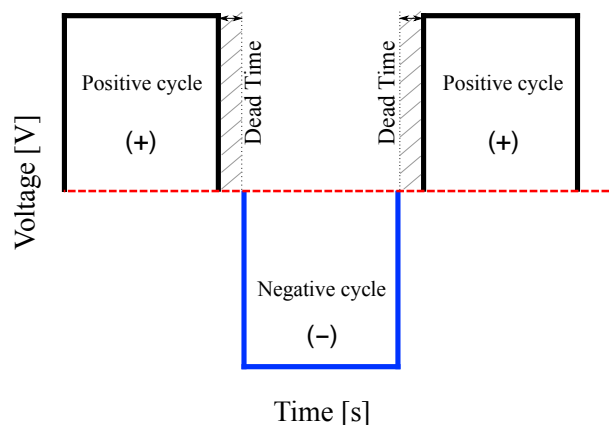


Figure 2. Balancing principle, output voltage of double-forward converter using dead time.

### 3. Operational Principle

In Figure 3, the implementation of the balancing circuit is schematically represented. Assume that the MOSFETs Q3 and Q4 are conducting, thus the primary receives a positive voltage. Through a rectifying Schottky diode, D2, and smoothing capacitor C7, cell 1 receives a DC voltage of the same polarity as the primary voltage. However, cell 2 will receive no voltage on its terminals since diode D3 is reverse-biased.

When the MOSFETs Q1 and Q2 are conducting, the primary receives a negative voltage and cell 2 receives a voltage of the opposite polarity. The MOSFETs Q1 to Q4 build up the full-bridge converter, supplying the signal to the primary.

They are driven by a self-oscillating full-bridge driver integrated circuit (IC). This IC receives its VCC from the battery pack voltage through resistor R6. This only occurs when MOSFET Q5 is conducting with a sufficiently high Gate-Source Voltage ( $V_{gs}$ ). This is achieved through the presence of resistor R7. The gate signal for the MOSFET Q5 originates from the optocoupler U2. There is a “bank select” to reduce the number of simultaneous signals. When receiving a bank select signal, the optocoupler U2 allows a collector-emitter current to flow and to pull up the gate of MOSFET Q5, thereby supplying the VCC of the driver.

As it is not preferable to disable the balancing in a short absence of a bank select signal (multiplexing), C5 holds up the gate of Q5 for a limited amount of time, sufficient for the downtime of the bank select. When the bank is critically imbalanced, or a surge current can flow, the polymeric positive temperature coefficient (PPTC) resettable fuse S1, in the form of a PPTC, will trip and primary current

will be limited by the “resettable fuse” and the LED driver/constant current regulator. When the voltage drop across the PPTC is too high the full-bridge driver will go into under-voltage lockout (typ.  $V_{CCUV} = 9\text{ V}$ ).

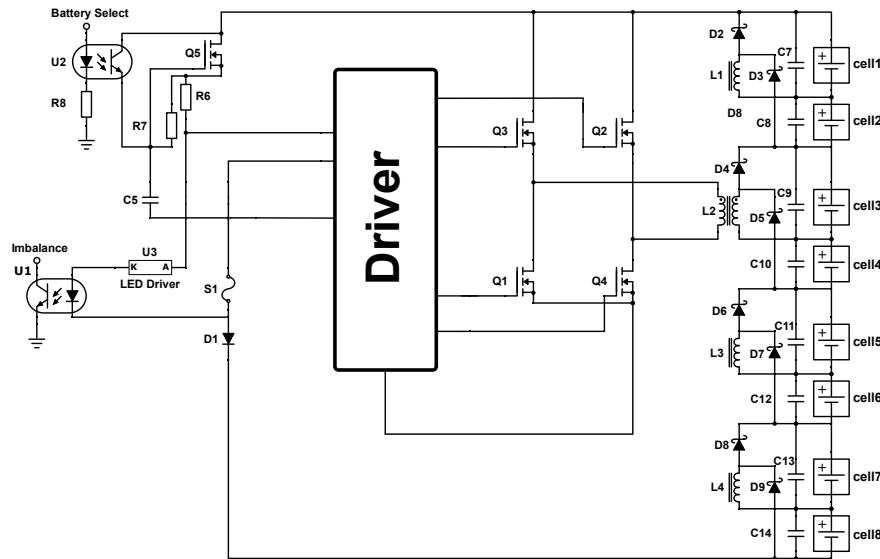


Figure 3. The simplified schematic of the proposed balancing circuit.

An imbalance (too low cell) indication occurs through optocoupler monitoring. When a significant imbalance occurs, the LED driver supplies enough current to the optocoupler U1 to notify the microcontroller that an imbalance has occurred. The pack could then be decoupled from the load to prevent further unbalancing. When the pack is charged again, it might recover and be used again. The capacitors C7 to C14 serve a double purpose.

They are smoothing capacitors as the inductance of wiring and circuit needs to be partly compensated by these capacitors, thus reducing the inductive drop and optimizing the increase of balancing current per voltage imbalance. The wiring inductance acts similar to an increased transformer leakage. The Diode D1 has the purpose to reduce possible circulating current. The selection of this added voltage drop follows from the proposed transformer winding ratio.

To evaluate the balancing current, consider the following configuration. In principle, the secondary balancing current is governed by the voltage imbalance and the leakage inductance of the transformer, by the following relation.

$$i_{balancing}(t) = \frac{1/n \times [(\sum_{i=1}^8 V_{bi}) - V_{D1}] - V_{Schottky} - V_{b'}}{L_{\sigma 2}} \times t \quad (1)$$

where  $0 \leq t < t_{on}$

$n$  = primary to secondary turns ratio

$i_{balancing}$  = Current of considered unbalanced cell

$V_{bi}$  = Voltage of cell  $i$

$V_{b'}$  = Voltage of considered unbalanced cell

$V_{D1}$  = Voltage drop of diode  $D_1$ .

$V_{Schottky}$  = Voltage drop of Schottky diode

$L_{\sigma 2}$  = Transformer leakage referred to the secondary.

$t_{on}$  = Balancing current rise time.

The average balancing current is obtained by taking into account the flyback or recovery time of the leakage inductance. The driver is provided with an internal dead time (DT), which is explained in the following section. As such

$$t_{on} = T/2 - DT \quad (2)$$

with  $T$  = period of the input signal.

The average balancing current is then given by

$$I_{balancing,average} = \frac{\frac{i_{balancing}(t_{on})}{2} \times (T/2 - DT + t_{off})}{T} \quad (3)$$

To obtain the flyback or recovery time of the leakage inductance, the recovery voltage during the dead time must be known.

$$V_{off} = -(V_{b'} + V_{Schottky}) \quad (4)$$

The recovery time is governed by the rate of current decrease and the peak current

$$t_{off} = L_{\sigma 2} \times i_{balancing}(t_{on}) / V_{off} \quad (5)$$

In the proof of concept, the balancing current is measured in function of the imbalance.

#### 4. Practical Implementation

In this section, an implementation of the proposed circuit is done, and the results are presented. One of the most critical components is the transformer. The winding ratio is determined out of the battery pack voltage according to the following reasoning. Assume that all cells are at nominal voltage, being 3.2 V. This causes a total battery pack voltage of  $V_{pack,nom} = 25.6$  V. Due to the limited forward voltage drop of the Schottky diodes, represented in Figure 4 the primary to secondary winding ratio,  $n$ , can be selected as (7.5).

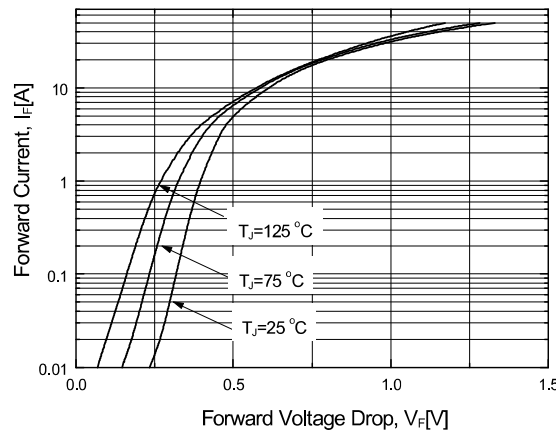


Figure 4. Forward characteristics of Schottky diode.

The peak voltage over a secondary winding at nominal battery cell voltage, neglecting primary side voltage drops and leakage inductance can be expressed as

$$V_{secondary,pk} = \frac{V_{pack,nom}}{n} = 3.413 \text{ V} \quad (6)$$

This gives a Schottky forward voltage drop of 0.213 V. Therefore, according to Figure 4, a circulating current can flow, but only at increased temperatures. This could result in some positive feedback during some time. The lowest voltage cell has the largest current, and will have the hottest diode. At a full charge cell voltage of 3.65 V, and thus a 29.2 V pack voltage, the forward voltage drop over the Schottky amounts to 0.243 V, which could lead to a more significant circulating current. To reduce the circulating current, an extra voltage drop is introduced in the form of diode D1 in

Figure 3. Assume that a 0.6 V diode voltage drop, therefore, the peak voltage over the secondary winding can be written as

$$V_{secondary,pk} = \frac{(V_{pack} - V_{diode})}{n} \quad (7)$$

By choosing another type of diode, or more diodes, the precise effect can be tuned. By doing this, no circulating current is present, both at full charge voltage and at nominal voltage. Only at elevated temperatures, a small circulating current appears. In the above-simplified argumentation for the transformer winding ratio, all primary side voltage drops, other than the diode drop, and all losses were neglected. Instead of attempting to model these, they will be evaluated in the experimental results section by experimental validation.

In the selection of the full-bridge driver, a possible saturation of the transformer core must be taken into account. In a balanced pack, there is no risk of saturation, since the peak flux density stays well below 0.3 T. In an unbalanced cell situation, there is a flux imbalance between positive and negative half-cycles, with a 50% duty ratio ( $\delta$ ). The unbalanced cell will require a charge and thus a current to balance, while another cell will not require this balancing charge.

Assume the positive half-cycle is the balancing cycle. During this positive half-cycle, a voltage drop and thus a flux drop occurs due to surrounding circuit components. The subsequent negative half-cycle will not have this flux drop and might, over a certain time, saturate the core. Thus, it needs a transformer core reset. A solution for this was found in a self-oscillating full-bridge driver IC with an internal dead time (DT) of 1  $\mu$ s. Depending on the extent of the imbalance and the corresponding balancing current, the core can demagnetize during this dead time.

As an argumentation for this selection, a simplified estimation of the required recovery time is given through a calculation example, performed on a transformer equivalent L-scheme, shown in Figure 5 based on measured and estimated values. Please note that this is a rough estimation simply to give an order of magnitude. The inductances were measured at the operating frequency. Since the leakage inductance (5.8  $\mu$ H) at the primary side is small compared to the magnetizing inductance (377  $\mu$ H), and the primary is wound close to the core, the use of a simplified L-scheme is allowed. In a symmetric T-scheme, primary and secondary leakages would have to be appropriately attributed to each winding.

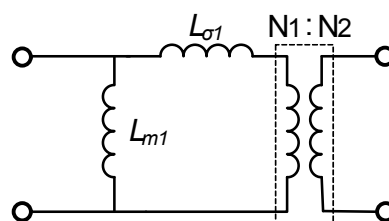


Figure 5. The equivalent L model of the transformer.

The required values are represented in Table 1.

Table 1. Calculation parameters.

Parameters	Values
f	67 kHz
$\delta$	50%
DT	1 $\mu$ s
$L_{\sigma1} = L_{\sigma1} + L'_{\sigma2} + L_{Layout}$	6.4 $\mu$ H
$R_1$	100 m $\Omega$
$R_2$	5 m $\Omega$
$R_{DSon}$	400 m $\Omega$

The leakage inductance ( $L_{\sigma 1}$ ) is the sum of the total transformer leakage referred to the primary ( $\Lambda_{\sigma 1} + \Lambda'_{\sigma 2}$ ) and the inductance of the printed circuit board (PCB) layout. The PCB layout inductance is measured using an LCR meter, by subtracting the leakage inductance, measured at the primary from the inductance measured with a shorted Schottky diode and output capacitor.  $R_1$  is a conservative estimate of the primary resistance, located on the left-hand side of the magnetizing inductance in the L-scheme. The DC resistance is estimated as follows:

$$R = MLT \times 15 \times \rho_{Cu} / A = 28.12 \text{ m}\Omega \quad (8)$$

$MLT$  = mean length of turn

$\rho$  = resistivity of copper (25 °C)

$A$  = wire cross-section area

However, there is also skin effect to take into account for the AC resistance. The skin depth is can be expressed as

$$\delta = \sqrt{\frac{2 \times \rho}{(2 \times \pi \times f \times \mu_r \times \mu_0)}} = 0.25 \text{ mm} \quad (9)$$

Since there is also a proximity effect and a DC component, a conservative estimate of 100 m $\Omega$  is assumed. Also,  $R_2$  was obtained following a similar reason.  $R_{DSon}$  is the total drain-source on-state resistance of the 2 switched MOSFETs. This value was obtained from the data sheet taking into account the temperature of 120 °C and amounted to 400 m $\Omega$ . As a reference, a severe imbalance is considered, with a peak primary current of 2 A ( $I_{peak}$ ).

This amounts to a peak balancing current of 15 A, which corresponds to a critically unbalanced pack. In reality, this current is very unlikely, due to the limiting influence of the PPTC and the imbalance that would have to be present. In addition, if it happens, the PPTC protects. In the proof of concept, a realistic balancing curve is presented.

In this worst-case, a simplified calculation to estimate the required dead time foreseen in the driver is given below. The flux linkage leakage field corresponding to a 2 A  $I_{peak}$ , neglecting magnetizing current can be expressed as

$$\Psi_{\sigma 1} = I_{peak} \times L_{\sigma 1} = 12.8 \text{ }\mu\text{Vs} \quad (10)$$

At an input voltage ( $V_{in}$ ) of 25 V, and following the previous argumentation regarding balancing current, this gives an unbalanced cell of about 2 V. The required flyback time for this leakage flux linkage is

$$\Delta t_{flyback} = \frac{\Psi_{\sigma 1}}{V_{off} \times n} = 0.525 \text{ }\mu\text{s} \quad (11)$$

The DC voltage drop at the output, compared to a no-load situation, corresponding with this leakage is

$$\Delta V_L = \frac{\Psi_{\sigma 1}}{[(T/2 - DT) \times n]} = 0.264 \text{ V} \quad (12)$$

The primary resistive voltage drop is estimated as follows

$$\Delta V_R = (R_1 + R_{DSon}) \times I_{peak} / 2 = 0.5 \text{ V} \quad (13)$$

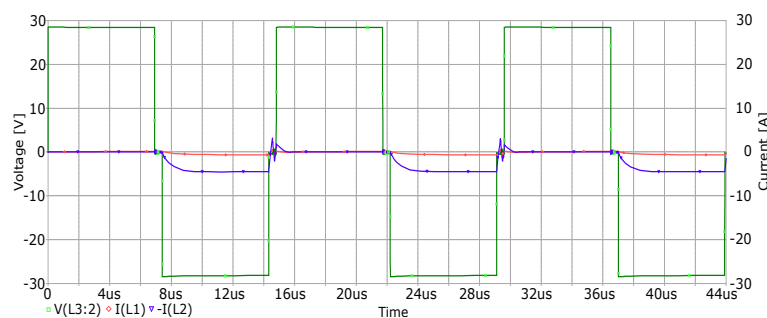
The factor 2 originates from the simplification of a linearly increasing current with a peak value of 2 A (normally an exponential behavior with  $\tau = L/R$  is expected). To obtain the voltage drop over the half-cycle, this peak drop can be halved. The recovery time required for this to obtain Vs-balance is

$$\Delta t_R = \frac{\Delta V_R \times (T/2 - DT)}{V_{off} \times n} = 0.13 \text{ }\mu\text{s} \quad (14)$$

According to the previous argumentation, the magnetizing current has  $0.34 \mu\text{s}$  time to get to zero in the  $1 \mu\text{s}$  dead time. From this rudimentary estimate, a  $1 \mu\text{s}$  dead time seems sufficient.

## 5. Simulation

To verify the previous assumptions, first, a simplified model including the transformer was build using the Cadence PSpice A/D circuit simulator. Two cells are modeled, with the source being modeled by two inverse (PWM) sources to control the dead time. In Figure 6 the set dead time was  $500 \text{ ns}$  to see if an imbalance in the waveform arises, thus indicating a possibility to saturate. The following waveforms are obtained, with the primary current in red color, the secondary current in blue color and the primary voltage in green color. This is in the case of an extreme imbalance.



**Figure 6.** Simulation results of two cells, primary voltage (green), primary current (red) and secondary current (blue).

No current imbalance perpetuates over the different periods. The resistive drop is present in the negative half-cycle. In Figure 6, the primary current, which includes the magnetizing current, can be seen. Even with a  $500 \text{ ns}$  dead time, the primary current has sufficient time to reset. The  $1 \text{ ms}$  internal dead time of the driver must suffice. The use of multilayer ceramic capacitors on the output is needed because of the bad frequency-dependent behavior of electrolytic capacitors, becoming high-impedance at the used frequencies. The multilayer ceramic capacitors are better in this regard, although displaying a reduced capacitance at the applied DC voltage offset ( $52 \text{ mF}$  at  $3 \text{ V}$  DC offset for a  $100 \mu\text{F}$  capacitor). They exhibit a very low ESL (Equivalent Series Inductance) and ESR (Equivalent Series Resistance) and low leakage, which is beneficial for the efficiency of the circuit. In the following section, the importance of the PCB layout on the balancing performance of the circuit will be quantified through measurements.

To testify the proposed circuit, the simulation results of the proposed circuit with MATLAB software are expressed. The switches are N-channel MOSFETs with body diodes and they are triggered by pulse width modulation (PWM), created by a pulse generator with a synchronous pattern. The switching frequency is  $67 \text{ kHz}$  with the duty ratio of  $45\%$ . The batteries are modeled with the capacitors with a value of  $50 \text{ mF}$ .

To apply cell imbalances, the battery pack with different cell voltages was considered. The cell voltages vary from  $3.1 \text{ V}$  to  $3.6 \text{ V}$  to apply the significant voltage differences. In Figure 7 the cell-balancing simulation results of the proposed transformer balancing circuit are presented. It can be seen in the Figure 7 that all cells are equalized and converged at the end of the balancing period. Therefore, the proposed equalization technique can balance all the neighboring cell voltages of the battery string to the same voltage level. The voltage difference of the lower cell to the higher cell is  $16.12\%$ . During the first test, the battery cells were not connected to the load.

The transformer primary and secondary voltage waveforms in steady state are shown in Figure 8. It can be noticed that all secondary voltages are at the same level which means all cells are balanced. The transformer has 4 secondary windings (S1–S4) per 8 cells. It can be seen that the average voltage is zero.



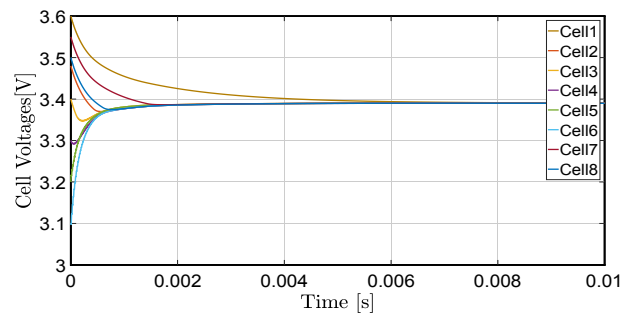


Figure 7. The simulation results of the proposed transformer balancing circuit.

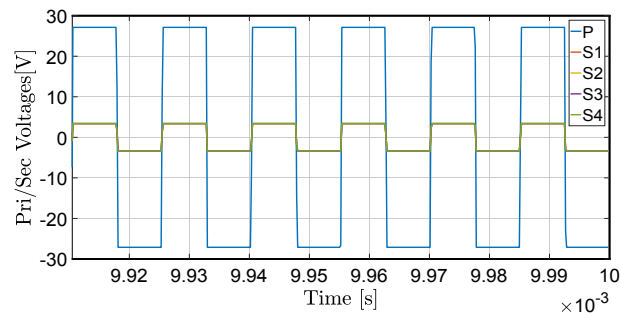


Figure 8. The transformer primary and secondary voltage waveforms in steady state.

To test the circuit with the load, a  $60\ \Omega$  resistor is connected to the total battery pack resulting in 0.5 A current and the simulation results are shown in Figure 9. It can be seen in the figure that all cells are equalized, and the total battery charge increased due to the dissipation through the resistor. It can be noticed that the circuit is robust against the load.

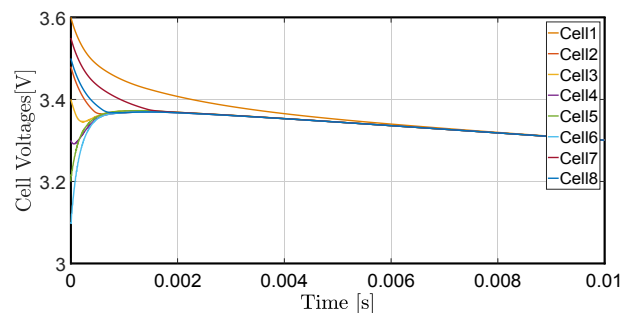


Figure 9. The simulation results of the proposed transformer balancing circuit with a load.

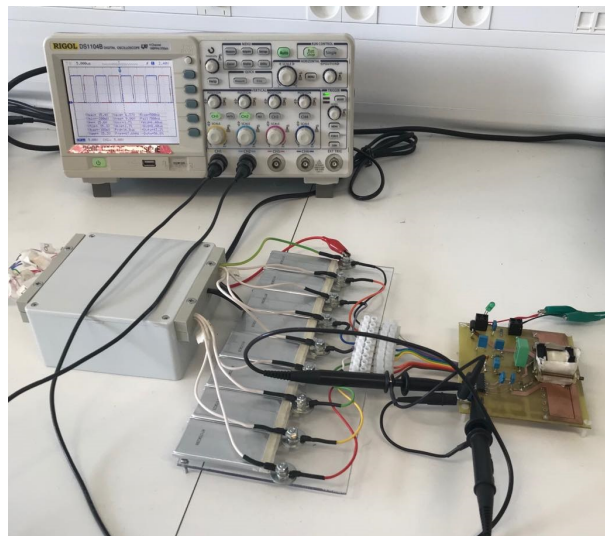
## 6. Experimental Results

To evaluate the properties of the proposed circuit concept, a testing PCB setup with two layers was constructed. To assure the induced voltages in each of the secondaries would be equal and the transformer is correctly wound, the magnetizing inductance is measured for the primary and each of the secondaries. If it is done correctly, the ratio of both would have to be  $n^2$ . In Table 2 the magnetizing inductance ratio for each of the secondary windings is presented.

Table 2. Magnetizing inductance ratio for each of the secondary windings.

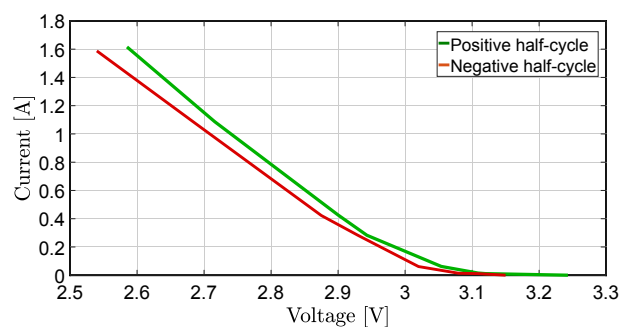
Parameters	Values
$L_{m1}$	56.2 $\mu\text{H}$
$L_{m2}$	56.21 $\mu\text{H}$
$L_{m3}$	56.21 $\mu\text{H}$
$L_{m4}$	56.2 $\mu\text{H}$

The photograph of the experimental set up of the proposed transformer balancing circuit is presented in Figure 10.



**Figure 10.** The photograph of experimental setup of the proposed transformer balancing circuit.

In the previous sections, some calculations were driven to estimate the amount of dead time that would be required to avoid saturation. However, the voltage drops obtained in these calculations are not accurate. Therefore, the characteristic of cell voltage vs balancing current is measured. Since it is not preferable to purposely unbalance battery cells before usage, the test is done by supplying the circuit with 25.6 V using a DC source. The imbalance is simulated by attaching different loads to the circuit terminals in the form of resistors. The result is shown in Figure 11. It can be observed that at small imbalances the balancing current is limited. A cell at 3.15 V, with the overall pack voltage being 25.6 V, gives a balancing current of 0.32 mA to that cell in a positive half-cycle. Therefore, there is little risk of unbalancing the pack outside of the final voltage regions.



**Figure 11.** Voltage vs balancing current (experimental result).

There is a small, but noticeable difference in the characteristic between positive and negative half-cycle balancing. As the duty ratio is almost symmetrical, this difference is most likely caused by a difference in impedance, caused by an asymmetry in the PCB or the measuring setup. The balancing characteristic can be defined by a balancing amperage per voltage imbalance for higher currents. For the positive half-cycle this amounts to  $3.33 \text{ A/V}_{\text{imbalance}}$ , for the negative half-cycle this amounts to  $2.57 \text{ A/V}_{\text{imbalance}}$ .

To emphasize the importance of the design on the balancing characteristic, these values are compared to a previous design, where less attention was given to the inductance of tracks and wiring. As described in the previous section, the layout inductance was measured for each of the designs. In the testing phase of the design, the primary current is limited by the PPTC to avoid damage. In further stages,

the trip current of the PPTC can be selected higher to allow balancing at higher currents. Since the trip current of the PPTC is 0.2 A, the balancing current is normally limited to 1.5 A ( $23\text{ }^{\circ}\text{C}$ ,  $t_{\text{trip}} = 4\text{ s}$ ). In this design, this corresponds to an imbalance of about 0.6 V. To evaluate the current limiting performance of the PPTC, the secondary current is measured at an imbalance that should trip the PPTC. However, 10 s already allows supporting the weaker cells a bit during an acceleration. The result is shown in Figure 12.

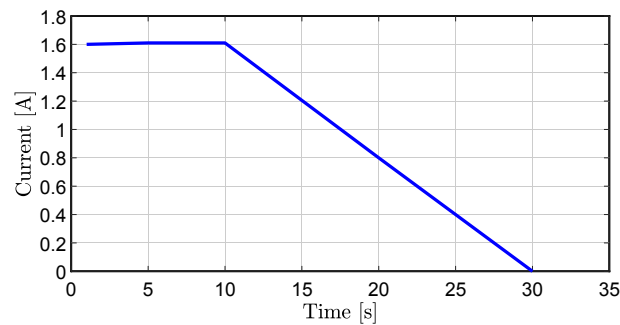


Figure 12. Current limiting performance PTC.

To protect the switching components and Schottky diodes from over-current, the PPTC should be over-dimensioned at a sufficiently low trip current, compared to the maximum ratings, due to its thermal inertia. The pulse width modulation (PWM) signals applied to the gate to source of the transistors are shown in Figure 13.

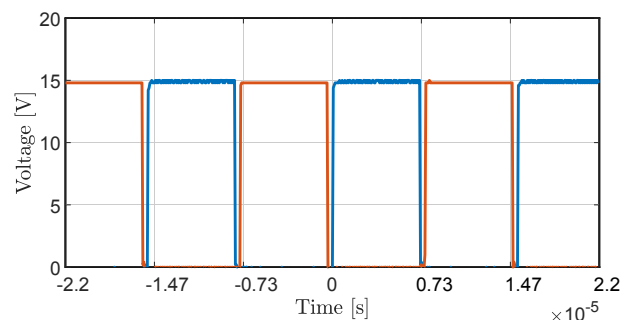


Figure 13. The gate to source voltages to the MOSFETs.

The blue signal is applied to Q3 and Q4, while the red signal is applied to Q1 and Q2. The primary and secondary voltage waveforms are represented in Figure 14, with a frequency of 67.6 kHz and the duty cycle of 50%.

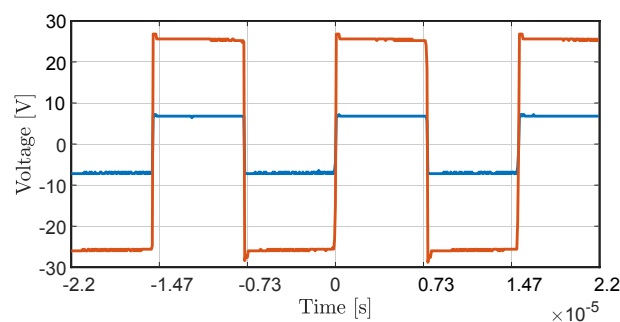


Figure 14. Primary (Red), and secondary (Blue) voltage waveform of the proposed circuit.

The transient behavior is due to the various parasitic capacities around the circuit charging up when the MOSFETs turn off. When the MOSFETs turn back on, these discharges cause current spikes. The behavior at the fall side of the balancing cycle assures Volt-second balance, as explained before.

Please note that at this imbalance the PPTC has already increased in resistance, thereby limiting the balancing current. To verify the proposed circuit, the battery cells with different voltage values were tested. The cell voltages vary from 2.7 V to 3.65 V to have imbalanced cells. First, the discharging process of the cells without a balancing circuit was investigated. The discharging results of the cell are presented in Figure 15.

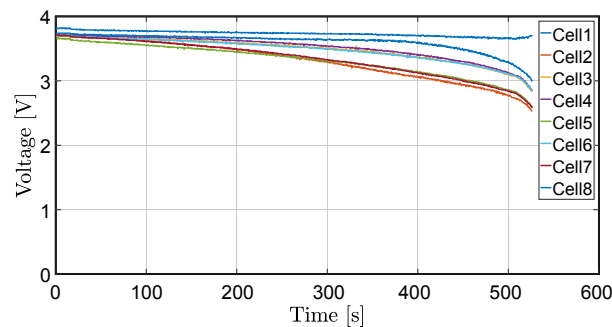


Figure 15. The discharging process of the cells without balancing circuit.

As it can be seen in the figure, the cell voltages are not converged and there are a significant voltage differences, because the balancing circuit is not presented. Then the discharging progress of the cells with the balancing circuit was examined. In Figure 16 the discharging results of the cells with the proposed circuit are presented. It can be seen that the cell voltage is converged due to the balancing circuit.

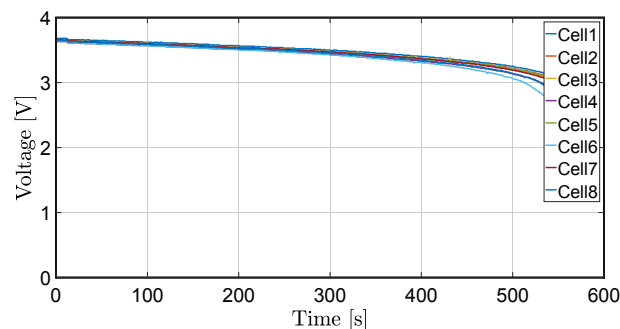


Figure 16. The discharging process of the cells with balancing circuit.

To verify the proposed circuit the circuit was tested with cell voltages from 2.7 V to 3.65 V to apply voltage differences. The cell voltage waveforms of the battery cells of the proposed circuit after balancing are presented in Figure 17.

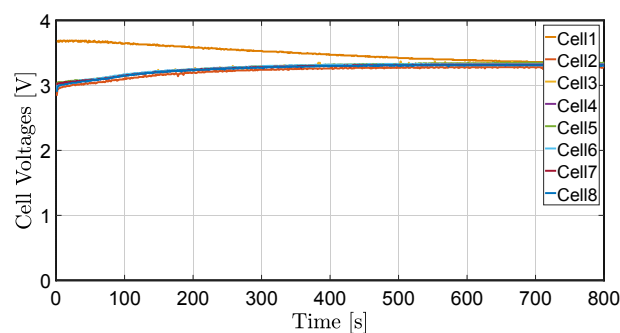
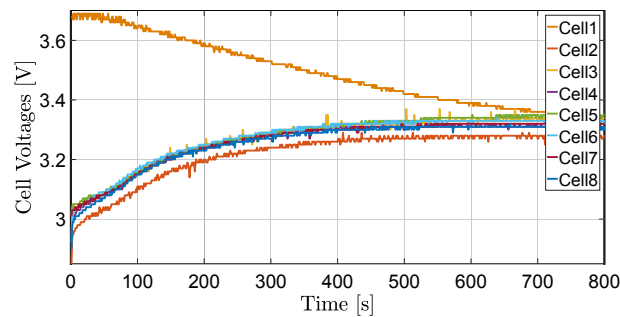


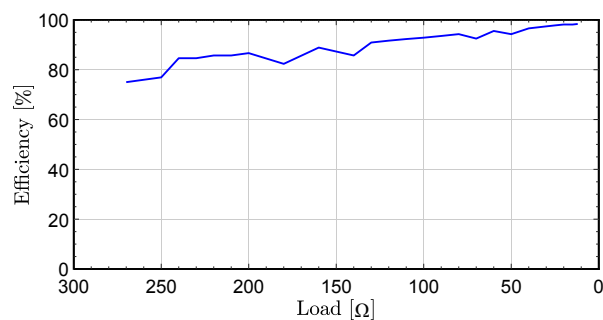
Figure 17. The cell voltage waveforms of the proposed circuit (cell 1 to cell 8).

In Figure 18 the cell voltage waveforms of the battery cells of the proposed circuit in closer view are presented. The voltage differences are significant, but they are equalized at the end.



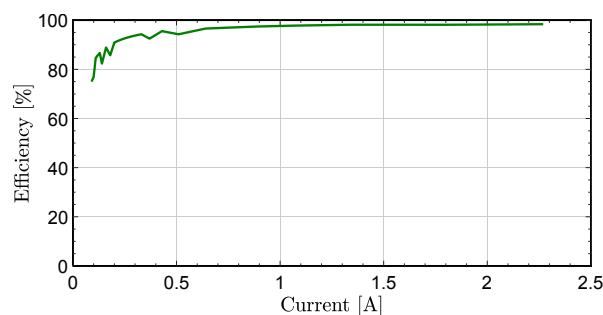
**Figure 18.** The cell voltage waveforms of the proposed circuit in closer view.

The efficiency of the proposed circuit was calculated by applying different loads at the output. The loads vary from  $270\ \Omega$  to  $12\ \Omega$ . The result of the efficiency versus loads is shown in Figure 19. It can be seen in the figure that with the load value of  $12\ \Omega$  the maximum efficiency is achieved.



**Figure 19.** The efficiency Vs loads of the proposed circuit.

In Figure 20, the efficiency of the proposed circuit versus output currents is presented. The output currents vary from 90 mA to 2.27 A. It can be noticed that at the current of 2.27 A the maximum efficiency is achieved.



**Figure 20.** The efficiency Vs output current of the proposed circuit.

## 7. Conclusions

In this paper, a multi-winding transformer cell-balancing based on a double-forward converter is proposed. Battery equalization is very important to enhance the battery life cycle and to maintain the total storage capacity and providing safe operation. If the multi-winding transformer is sufficiently symmetrical, the circuit can achieve favorable balance voltage. This method is especially implemented for a lithium-ion battery string of eight cells. The energy is transferred by a double-forward converter. Compared to the common methods, this scheme reduces the required number of secondaries by a factor of two, resulting in small size and low cost. The proposed circuit also uses a full-bridge driver that controls four N-channel MOSFETs as switches, which means two times fewer transistors than cells, resulting in less switching losses. The experimental results and simulation have shown the proposed equalizer demonstrates a good and competitive overall performance in terms of the equalization

speed, efficiency, and complexity of implementation. Furthermore, this method is suitable for electrical vehicle, hybrid electrical vehicle applications and grid-connected battery applications.

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## Abbreviations

The following abbreviations are used in this manuscript:

BOM	Bill of materials
EMF	Electromotive force
EV	Electric vehicles
ES	Electric scooters
DT	Dead time
HEV	Hybrid electric vehicles
LCR meter	Inductance (L), capacitance (C), and resistance (R) meter
LED	Light-emitting diode
MATLAB	Matrix laboratory
MLT	Mean length turn
MOSFET	Metal–oxide–semiconductor field-effect transistor
PCB	Printed circuit board
PPTC	Polymeric positive temperature coefficient
PWM	Pulse Width Modulation
SOC	State of charge
UPS	Uninterruptible power supplies

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